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DRY ETCHING PROCESS FOR COMPOUND SEMICONDUCTORS

TECHNICAL FIELD

[0001] This invention relates to a dry etching process for semiconductor wafers. More particularly, the present invention relates to a dry etching process that selectively etches a compound semiconductor wafer faster than the front-side metal layer. Further, the dry etching process produces a vertical wall profile on the compound semiconductor wafer without undercutting the top of an opening.

BACKGROUND ART

[0002] Semiconductor wafer processing technologies including Gallium Arsenide (GaAs) and Indium Phosphide (InP) require improvements such as increased etching selectivity for a compound semiconductor wafer compared to a front-side metal layer. For example, as shown in Figure 1, the thickness varies across a compound semiconductor wafer.

[0003] As such, to prevent punch-through of the compound semiconductor wafer to the front-side metal layer, a dry etching process needs to selectively etch the backside of the compound semiconductor wafer. Figure 1 is an illustration showing a thickness difference across the compound semiconductor wafer. Specifically, Figure 1 shows a ten micron thickness difference across the compound semiconductor wafer whereby a edge 6 thickness is within the range of approximately 60 μm to approximately 80 μm and a center 8 thickness is within the range of approximately 70 μm to approximately 90 μm. The creation of a via-opening in both edge 6 and center 8 of the compound semiconductor wafer requires complete etching through both center 8 and edge 6 without punching-through the front-side metal layer, i.e., etching wafer front-side metal layers 9A, 9B on a portion of the wafer.

[0004] Presently available etching processes are not selective enough to prevent punch-through of the front-side metal layer. As such, there is a need for a dry etching process that selectively etches the backside of the compound semiconductor wafer over the front-side metal layer, thereby preventing the front-side metal layer punch-through, even with compound semiconductor material thickness variations across the wafer, as well as providing other advantages over present etching processes, such as realizing an opening with vertical sidewalls, no undercutting the via-opening, and making a repeatable process.

DISCLOSURE OF THE INVENTION

[0005] Accordingly, the present invention provides a dry etching process for a compound semiconductor wafer that prevents front-side metal layer punch through with large thickness variations across the compound semiconductor wafer. Other advantages include that the dry etching process creates an opening with vertical sidewalls in both X and Y crystalline directions and creates no undercutting of the top of the opening. In one embodiment of the present invention, the compound semiconductor wafer comprises a compound semiconductor material. As disclosed, the present invention is a dry etching process for the compound semiconductor material comprising the steps of placing in a chamber the compound semiconductor material having an exposed portion, adding a halogen etchant, adding a nitrogen gas to the chamber, and heating the electrostatic chuck that supports the compound semiconductor material.

[0006] Afterwards, applying bias power and a pulse-modulated power to the controlled amount of the gas, whereby the exposed portion of the compound semiconductor material is etched with vertical sidewalls. This process creates within a range of approximately 70 times greater etch rate to approximately 80 times greater etch rate for the compound semiconductor material than the etch rate of the deposited front-side metal layer.

[0007] In one embodiment, the halogen etchant is a halogen gas is selected from a group consisting of Chlorine, Fluorine and Bromine. Further, in one alternative embodiment, the halogen etchant comprises a halogen-containing compound selected from the group consisting of Hydrogen Bromide and Hydrogen Iodide.

[0008] In the embodiment, the etching process further includes heating, biasing and pulse-modulated powering the halogen etchant and the nitrogen gas within the chamber to complete

the etching process. It is an advantage of the present invention that the dry etching process does not damage a non-exposed portion of the compound semiconductor wafer during the etching process. It is an additional advantage of the present invention that the addition of the nitrogen gas to the halogen etchant reduces the etch rate of the front-side metal layer by more than 90 percent.

[0009] Additionally, the present invention discloses the dry etchant for compound semiconductor material G and F, wherein G is selected from the group consisting of a halogen gas and a halogen-containing compound, and F is a nitrogen gas, and wherein G and F volume ratio is selected from a range of approximately 10:1 to approximately 12:1. In this embodiment of the present invention, the halogen gas is one selected from the group consisting of Chlorine, Fluorine and Bromine and the halogen-containing compound is one selected from a group consisting of Hydrogen Bromide (HBr) and Hydrogen Iodide (HI).

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a better understanding of the present invention, reference is made to the below-referenced drawings. Reference numbers refer to the same or equivalent parts of the present invention throughout the several figures of the drawings.

[0011] Figure 1 is a diagram displaying the thickness variation across a compound semiconductor wafer.

[0012] Figure 2A is a beginning structure for the dry etching process for a compound semiconductor material.

[0013] Figure 2B depicts the inventive dry etching flow process for a compound semiconductor material.

[0014] Figure 2C is a final structure for the dry etching process for a compound semiconductor material.

[0015] Figure 3 is an example of the present invention illustrating the Figure 2B dry etch process of the present invention for a compound semiconductor wafer resulting in no undercutting and no front-side metal layer punch-through.

MODES FOR CARRYING-OUT THE INVENTION

[0016] Figures 2A, 2B and 2C illustrate a beginning structure, a process flow, and a final structure disclosing a dry etching process for a compound semiconductor material. In one embodiment, compound semiconductor wafer comprises a compound semiconductor material. More specifically, the dry etching process described below is one that prevents front-side metal layer punch-through even with large thickness variations across the compound semiconductor material.

[0017] Figure 2A depicts the compound semiconductor material that will be etched using the inventive dry etching process. In particular, the inventive dry etching process comprises the step of placing in a chamber (not shown in the Figure) the compound semiconductor material 18 on an electrostatic chuck (not shown in the Figure). Preferably, the chamber is an inductively coupled plasma (ICP) power machine such as a Trikon Omega 201 ICP. The structure in Figure 2A comprises a compound semiconductor material 18 having exposed portions 20A, 20B. In this step, the compound semiconductor material 18 is selected from a group consisting of Gallium Arsenide (GaAs), Indium Phosphide (InP) and III-V semiconductor compound. Further, at least one portion of compound semiconductor 18 is covered by masks 22A, 22B. In one embodiment, masks 22A, 22B, 22C are photo-resist layers. In the embodiment of this present invention, front-side metal layers 16A, 16B comprise gold (Au). In another embodiment, front-side metal layers 16A, 16B may further comprise titanium, platinum or other materials that allow electrical conductive properties for electrical current flow.

[0018] Figure 2B depicts the inventive dry etch flow process. Afterwards in this embodiment, a halogen etchant 24 selected is a halogen gas. In one alternative embodiment, halogen etchant 24 is a halogen gas selected from a group consisting of Chlorine, Fluorine and Bromine. Further, in another alternative embodiment of the present invention, halogen-containing compound is selected from a group consisting of Hydrogen Bromide (HBr) and Hydrogen Iodide (HI). Following, halogen etchant 24 is released 26 into the chamber (not shown in the Figure). Following nitrogen gas 28 is added to the chamber. Preferably, the volume ratio of halogen etchant 24 to nitrogen gas 28 is greater than 10:1. Furthermore, in an alternate embodiment of the present invention, the volume ratio of halogen etchant 24 to nitrogen gas 28 is selected from a range of approximately 10:1 to approximately 12:1.

[0019] Afterwards, applying heating step 30 comprising heating the electrostatic chuck to a temperature selected from the range of approximately 130 degrees C to approximately 170 degrees C. In this same embodiment, pressurizing step 32 for halogen etchant 24 and nitrogen gas 28 selected from a range of approximately 5 milli-Torr to approximately 20 milli-Torr. Following, applying a bias power 34 and pulse-modulated power 35 to halogen etchant 24 and nitrogen gas 28. Preferably, bias power step comprises applying bias power 34 to the semiconductor material which preferably is a 4 inch radius semiconductor wafer. Preferably, bias power 34 is selected from a range of approximately 20 Watts to approximately 50 Watts. For other semiconductor substrates, applied bias power 34 scales to maintain the above described ratio of Watts to surface area of the semiconductor wafer. Furthermore, pulse-modulated power 35 comprises applying an inductively coupled plasma (ICP) power source to semiconductor material 18 selected from a range of approximately 350 Watts to approximately 750 Watts. Preferably, ICP power source is a Trikon Omega 201 ICP.

[0020] Figure 2C is a final structure resulting from the dry etching process of the present invention. In this Figure, the exposed portion of the compound semiconductor material is etched with vertical sidewalls in the X crystalline direction 38 and Y crystalline direction 40 showing no punch-through of front-side metal layers 16A, 16B.

[0021] Figure 3 is an example illustrating the dry etching flow process of Figure 2 of the present invention of a compound semiconductor wafer. In this Figure 3 based on a Scanning Electronic Microscope (SEM) photograph, a compound semiconductor material is dry etched using the flow process of Figure 2B resulting in no undercutting 46 and no punch-through shown on the SEM front-side metal layer 50. As shown, there is no undercutting 46 of SEM via-opening or punch-through of SEM front-side metal layer 50. In this embodiment of the present invention, SEM via hole width 52 may be in a range of approximately 60 microns (μms) to approximately 70 μms. Further, in this same embodiment of the present invention, SEM via hole height 54 may be for the edge of the wafer in a range of approximately 60 μms to approximately 70 μms. In addition, in this same embodiment of the present invention, the SEM via hole height 54 may be for the center of the wafer in a range of approximately 70 μms to approximately 90 μms.

[0022] It is an advantage of the present invention that the dry etching process does not damage the non-exposed portion of the compound semiconductor wafer during the etching process. It is an additional advantage of the embodiment of the present invention that the addition of nitrogen gas to halogen etchant 24 reduces the etch rate of a front-side metal layer with a range of approximately 80 percent to approximately 90 percent compared to the etch rate of the compound semiconductor material.

[0023] Additionally, the present invention discloses the dry etchant for compound semiconductor material G and F, wherein G is selected from the group consisting of a halogen etchant 24 and F is a nitrogen gas 28, and wherein the volume ratio of G to F is with a range of approximately 10:1 to approximately 12:1. In this same embodiment of the present invention, halogen etchant 24 is a halogen gas selected from a group consisting of Chlorine, Fluorine and Bromine. In the alternative, halogen etchant 24 is a halogen-containing compound selected from a group consisting of Hydrogen Bromide (HBr) and Hydrogen Iodide (HI).

[0024] Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention and the present embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims.

[0025] Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, one skilled in the art should recognize that various changes and modifications in form and material details may be made without departing from the spirit and scope of the inventiveness as set forth in the appended claims. No

claim herein is to be construed under the provisions of 35 U.S.C. § 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."

INDUSTRIAL APPLICABILITY

[0026] The present invention applies industrially to dry etching process for semiconductor wafers. More particularly, the present invention applies industrially to a dry etching process that selectively etches a compound semiconductor wafer faster than the front-side metal layer. Even more particularly, the present invention, applies industrially to the dry etching process produces a vertical wall profile.